Claims

What is claimed is:

1. A method of establishing electrical communication between a first device and a second device in a semiconductor circuit, comprising:

contacting said first device with a first end of an electrically conductive material;

layering an initial barrier component over a second end of said electrically conductive material;

nitridizing at least a portion of said initial barrier component; and

contacting said second device with said portion of said initial barrier component.

2. The method in claim 1, further comprising a step of siliciding at least a second portion said initial barrier component.

3. The method in claim 2, wherein said step of contacting said first device further comprises contacting a transistor with doped silicon; and wherein said step of contacting said second device further comprises contacting a capacitor.

4. The method in claim 3, wherein said step of contacting said second device further comprises contacting a capacitor with a doped polysilicon plug.

5. A method of processing a semiconductor circuit on a substrate covered with an insulating layer, wherein said layer defines an opening over said substrate, and polysilicon contacts a surface of said substrate and a bottom of said opening; and wherein said method comprises:

providing an initial barrier component on at least said polysilicon; and

nitridizing said initial barrier component.

6. The method in claim 5, further comprising siliciding said initial barrier component.

7. The method in claim 6, further comprising a step of providing an oxidation protection layer within said opening.

8. The method in claim 7, further comprising a step of recessing said polysilicon.

9. The method in claim 8, wherein said step of providing an initial barrier component further comprises providing said initial barrier component only on said polysilicon.

10. The method in claim 9, wherein said step of providing said initial barrier component comprises depositing said initial barrier component through selective chemical vapor deposition.

11. The method in claim 9, wherein said step of providing said initial barrier component further comprises the steps of:

depositing said initial barrier component on said polysilicon and within said opening; and

etching said initial barrier component within said opening.

12. A method of preparing a semiconductor device comprising a container defined by at least one insulation layer, comprising:

forming a poly plug extending toward said container and having a surface under said container;

depositing an initial barrier component at least between said poly plug and said container; and

nitridizing a first portion of said initial barrier component, wherein said first portion is next to said container.

13. The method in claim 12, further comprising a step of siliciding a second portion of said initial barrier component, wherein said second portion is between said poly plug and said first portion of said initial barrier component.

14. The method in claim 13, further comprising a step of depositing an oxidation protection layer within said container and over said first portion.

15. The method in claim 14, wherein said step of depositing an initial barrier component further comprises lining said container with said initial barrier component; and wherein said step of nitridizing a first portion of said initial barrier component further comprises nitridizing said initial barrier component lining said container.

16. A method of forming an interface between a transistor and a capacitor, wherein said transistor includes a doped portion of a substrate, and an in-process poly plug is supported by said doped portion and extends upward along a length to a capacitor site, and wherein said method comprises:

reducing said poly plug to generally half of said length;

selectively chemically vapor depositing a barrier component onto said poly plug, wherein said barrier component has a bottom next to said poly plug and a top opposite from said bottom; and

nitridizing said top of said barrier component.

17. The method in claim 16, wherein said step of nitridizing further comprises nitridizing generally half of said barrier component.

18. The method in claim 17, further comprising a step of siliciding said bottom of said barrier component.

19. The method in claim 18, wherein said step of siliciding further comprises siliciding generally half of said barrier component.

20. A method of interfacing a silicon contact with a semiconductor device, comprising:

forming a barrier to diffusion from said silicon contact using a first material layered

over said silicon contact; and

forming a barrier to oxidation of said silicon contact using a selection of said first material and a second material.

21. The method in claim 20, wherein said step of forming a barrier to oxidation further comprises providing a layer of ruthenium oxide.

22. The method in claim 20, wherein said step of forming a barrier to diffusion further comprises layering over said silicon contact a selection of platinum, iridium, osmium, palladium, rhodium, ruthenium, and oxides thereof; and wherein said step of forming a barrier to oxidation further comprises forming a barrier to oxidation using said selection.

23. The method in claim 20, wherein said step of forming a barrier to diffusion further comprises providing a metal nitride layer; and wherein said step of forming a barrier to oxidation further comprises providing a layer comprised of a selection of a metal or a metal oxide.

24. The method in claim 23, wherein:

said step of forming a barrier to diffusion further comprises providing a first layer selected from:

a nitride of titanium, tungsten, rhenium, and platinum-group metals,
an oxide of said platinum-group metals,
an alloy of said platinum-group metals, and
a boride of a transition metal; and

said step of forming a barrier to oxidation further comprises providing a second layer over said first layer, wherein said second layer is selected from platinum-group metals and an oxide of platinum-group metals.

25. A method of establishing electrical contact between a semiconductor substrate and a semiconductor device, comprising:

covering said substrate with an insulating layer;

etching a hole through said insulating layer to said substrate;

partially plugging said hole with doped polycrystalline silicon;

depositing at least one metal layer within said hole over said doped polycrystalline silicon;

nitridizing said at least one metal layer;

siliciding said at least one metal layer; and

forming said semiconductor device over said at least one metal layer.

26. The method in claim 25, wherein:

said step of depositing at least one metal layer comprises depositing a titanium layer;

said step of nitridizing said at least one metal layer comprises nitridizing said titanium layer; and

said step of siliciding said at least one metal layer comprises siliciding said titanium layer.

27. The method in claim 25, wherein:

said step of siliciding said at least one metal layer comprises siliciding a titanium layer;

said step of nitridizing said at least one metal layer comprises nitridizing a non-titanium layer; and

said step of forming said semiconductor device further comprises forming said

semiconductor device over said non-titanium layer.

28. The method in claim 27, wherein said step of nitridizing a non-titanium layer comprises nitridizing a tungsten layer.

29. A damascene process, comprising:

forming a first insulation layer over a semiconductor substrate;

forming a first hole in said first insulation layer;

forming doped polysilicon in said first hole; and

forming a silicon barrier over said doped polysilicon.

30. The process in claim 29, wherein said step of forming doped polysilicon further comprises forming doped polysilicon having a low surface within said first hole.

31. The process in claim 30, wherein said step of forming doped polysilicon having a low surface within said first hole further comprises:

generally completely filling said first hole with said doped polysilicon; and

etching a portion of said doped polysilicon.

32. The process in claim 31, further comprising a step of forming an oxygen barrier over said silicon barrier.

33. The process in claim 32, further comprising a step of forming an electrical contact enhancement layer under said silicon barrier.

34. The process in claim 33, further comprising:

forming a second insulation layer over said first insulation layer; and

forming a second hole in said second insulation layer, wherein said second hole is over said first hole.

35. The process in claim 34, wherein said step of forming an oxygen barrier further comprises forming an oxygen barrier extending into said second hole.

36. A method of processing a semiconductor device, comprising:

providing an silicon interconnect material contacting an electrically conductive first

portion of said semiconductor device; and

providing an initial barrier component contacting said interconnect material.

37. The method in claim 36, wherein said step of providing an initial barrier component further comprises initially protecting said semiconductor device against silicon diffusion.

38. The method in claim 36, wherein said step of providing an initial barrier component further comprises initially providing a component capable of protecting said semiconductor device against silicon diffusion after further processing.

39. The method in claim 38, further comprising nitridizing said initial barrier component; and wherein said step of initially providing a component further comprises providing a component capable of protecting said semiconductor device against silicon diffusion after being nitridized.

40. A method of preventing at least some diffusion from a conductive material in a semiconductor device, comprising:

surrounding a side of said conductive material with an insulator;

depositing a barrier material onto said conductive material; and

nitridizing said barrier material.

41. The method in claim 40, wherein said step of depositing a barrier material further comprises depositing said barrier material onto said conductive material and onto said insulator.

42. The method in claim 41, further comprising a step of removing said barrier material from said insulator.

43. A method of treating a silicon contact, comprising:

depositing a barrier component onto said silicon contact; and

nitridizing said barrier component.

44. The method in claim 43, wherein said step of depositing a barrier component further comprises siliciding said barrier component.

45. The method in claim 43, further comprising a step of discretely siliciding said barrier component.

46. The method in claim 45, wherein said step of discretely siliciding said barrier component further comprises siliciding at least an un-nitridized portion of said barrier component.

47. The method in claim 46, wherein said step of discretely siliciding said barrier component further comprises reacting said barrier component with silicon in said silicon contact.

48. The method in claim 47, wherein said step of reacting said barrier component further comprises reacting said barrier component with a portion of said silicon contact containing oxygen.

49. A memory cell, comprising:

a transistor;

a capacitor;

a silicon plug extending from said transistor toward said capacitor and physically separate from said capacitor; and

a diffusion barrier between said silicon plug and said capacitor.

50. The memory cell in claim 49, wherein said diffusion barrier is made of a metal nitride.

51. The memory cell in claim 50, wherein said diffusion barrier is made of titanium nitride.

52. The memory cell in claim 51, further comprising an un-nitridized layer of titanium between said diffusion barrier and said silicon plug.

53. The memory cell in claim 52, wherein said un-nitridized layer of titanium is a silicided layer of titanium.

54. The memory cell in claim 53, wherein said silicided layer of titanium is generally as thick as said diffusion barrier.

55. An interface between a poly plug and a storage node of a capacitor, comprising:

an electrical contact enhancement layer over said poly plug;

a silicon barrier over said electrical contact enhancement layer; and

an oxidation protection layer over said silicon barrier and contacting said storage node.

56. The interface in claim 55, wherein said electrical contact enhancement layer is a metal silicide layer; said silicon barrier is a metal nitride layer; and said oxidation

protection layer is a layer selected from metals, metal oxides, and metal alloys including platinum.

57. The interface in claim 56, wherein said electrical contact enhancement layer and said silicon barrier contain the same metal.

58. The interface in claim 56, wherein said electrical contact enhancement layer is of a form $TiSi_X$; and said silicon barrier is made of tungsten nitride.

59. A part of a semiconductor circuit including insulation over an electrically conductive surface, wherein said insulation defines an opening and a hole from said opening to said surface, wherein said part comprises:

a conductive material filling about half of said hole in said insulation, wherein said

conductive material contacts said surface; and

a diffusion barrier at least within said hole and over said conductive material.

60. The part in claim 59, wherein said diffusion barrier lines said opening.

61. The part in claim 60, further comprising an oxygen barrier conformal to said diffusion barrier.

62. A portion of a semiconductor device having an electrically conductive first element, an electrically conductive second element contacting said first element, and an electrically conductive third element configured to electrically communicate with said first element through said second element, wherein said portion comprises:

an oxidation barrier contacting said third element; and

a silicon diffusion barrier contacting said oxidation barrier and said second element;

wherein said oxidation barrier and said silicon diffusion barrier are configured to act as an electrical communication interface between said second element and said third element.

63. The portion in claim 62, wherein said oxidation barrier and said silicon diffusion barrier define a continuous iridium layer.

64. The portion in claim 62, wherein said oxidation barrier is made of ruthenium oxide; and said silicon diffusion barrier is also made of ruthenium oxide.

65. The portion in claim 64, wherein said oxidation barrier and said silicon diffusion barrier define a continuous ruthenium oxide layer.

66. An interconnect structure, comprising:

a doped polysilicon material having a shape defined by an underlying support structure and an adjacent insulative material;

an electrically conductive material over said doped polysilicon material and said insulative material; and

a silicon barrier between said doped polysilicon material and said electrically conductive material.

67. The structure in claim 66, wherein said silicon barrier contacts said doped polysilicon material and said electrically conductive material.

68. The structure in claim 66, further comprising an oxidation protection layer contacting and interposed between said silicon barrier and said electrically conductive material.

69. The structure in claim 68, further comprising an electrical contact enhancement layer contacting and interposed between said silicon barrier and said doped polysilicon material.

70. An interface for a semiconductor device including a poly plug contacting a substrate and a capacitor plate over said poly plug, comprising:

a diffusion barrier under said capacitor plate and over said poly plug, said diffusion barrier selected from a group consisting of:

titanium nitride,
tungsten nitride,
rhenium,
rhenium nitride,
a platinum-group metal,
a nitride of said platinum-group metal.
an oxide of said platinum-group metal,
an alloy of said platinum-group metal,
a boride of a transition metal, and
combinations of the above materials.

71. The interface in claim 70, further comprising an oxidation barrier under said capacitor, over said diffusion barrier, and comprising a selection of a platinum-group metal and an oxide of said platinum-group metal.

72. The interface in claim 71, further comprising an electrical contact enhancement layer under said diffusion barrier and over said poly plug, comprising a silicide material.